In the Claims:

Please cancel claims 44-47.

1   1. (Previously amended) A method of compiling a software program for a

2 programmable processor having a functional unit associated with at least two issue slots,

3 the method comprising:

4   receiving a set of processor-executable operations comprising a first processor-

5 executable operation of a type typically associated with at least two issue slots and a

6 second processor-executable operation; and

7   replacing the first processor-executable operation with a third equivalent

8 processor-executable operation associated with fewer than all of the issue slots, thereby

9 allowing one or more of the rest of the issue slots to be used by the second processor-

10 executable instruction.

1   2. (Previously amended) The method of claim 1, wherein replacing the first

2 processor-executable operation with a third equivalent processor-executable operation

3 further comprises analyzing the first processor-executable operation and external

4 information to determine whether the first processor-executable operation can be replaced

5 by the third equivalent processor-executable operation.

1   3. (Previously amended) The method of claim 1, wherein the third equivalent

2 processor-executable operation is associated with only one issue slot.

1   4. (Previously amended) The method of claim 1, wherein the third equivalent

2 processor-executable operation is associated with a plurality of issue slots.

1   5. (Previously amended) The method of claim 1, wherein replacing the first

2 processor-executable operation with a third equivalent processor-executable operation

3 further comprises:

4   determining a number of input registers and a number of output registers that are

5 used by the first processor-executable operation; and

6   when the first processor-executable operation uses at most two input registers and

7   one output register, replacing the first processor-executable operation with the third

8   equivalent processor-executable operation associated with only one issue slot.

1   6-7. (cancelled)

1   8. (Previously amended) The method of claim 1, wherein the first processor-

2   executable operation is a shuffle operation.

1   9. (Previously amended) The method of claim 1, wherein the first processor-

2   executable operation is a floating point operation.

1   10. (original) A method of compiling a software program for a programmable

2   processor having a functional unit associated with a plurality of issue slots, the method

3   comprising:

4   receiving a processor-executable superoperation of a type typically associated

5   with at least two issue slots;

6   determining a number of input registers and a number of output registers that are

7   used by the superoperation; and

8   when the superoperation uses at most two input registers and one output register,

9   replacing the superoperation with an equivalent processor-executable operation

10   associated with only one issue slot.

1   11. (original) The method of claim 10, further comprising:

2   identifying any source operations that produce a result affecting a result of the

3   superoperation;

4   placing commands for the source operations in instruction words;

5   selecting an earliest instruction word from a set of instruction words after the

6   instruction words in which commands for the source operations have already been

7   placed; and

8   determining whether an instruction word can be constructed that contains any

9   commands already included in the earliest instruction word in addition to a command for

10   the superoperation.

1   12. (original) The method of claim 11, further comprising:

2   when an instruction word that contains any commands already included in the

3   earliest instruction word in addition to the command for the superoperation cannot be

4   constructed, selecting a subsequent instruction word; and

5   determining whether an instruction word that contains any commands already

6   included in the earliest instruction word in addition to the command for the

7   superoperation can be constructed using the subsequent instruction word.

1   13. (original) The method of claim 10, wherein the superoperation is a shuffle

2   operation.

1   14. (original) The method of claim 10, wherein the superoperation is a floating

2   point operation.

1   15. (Previously amended) A method of executing a first instruction that is

2   typically associated with at least two issue slot by a processor having a functional unit

3   associated with a plurality of issue slots, the method comprising:

4   determining whether the first instruction can be executed using fewer than the at

5   least two issue slots; and

6   when the first instruction can be executed using fewer than the at least two issue

7   slots, replacing the first instruction with a second equivalent instruction associated with

8   fewer than the at least two issue slots thereby allowing one or more of the rest of the issue

9   slots to be used by a third instruction.

1   16. (cancelled)

1   17. (Previously amended) The method of claim 15, wherein determining whether

2   the first instruction can be executed using fewer than the at least two issue slots further

3   comprises:

4   determining a number of input registers and a number of output registers that are

5   used by the first instruction; and

6   when the first instruction uses at most two input registers and one output register,

7   replacing the first instruction with the second instruction, the second instruction being

8   associated with a single issue slot.

1   18-19. (cancelled)

1   20. (Previously amended) The method of claim 15, wherein the second

2   instruction is associated with two or more issue slots.

1   21. (Previously amended) The method of claim 15, wherein the first instruction is

2   a shuffle operation.

1   22. (Previously amended) The method of claim 15, wherein the first instruction is

2   a floating point operation.

1   23. (Previously amended) A processor-readable medium containing processor-

2   executable instructions for:

3   receiving a set of operations comprising a first operation of a type typically

4   associated with at least two issue slots of a functional unit of a programmable processor

5   and a second operation; and

6   replacing the first operation of the type typically associated with at least two issue

7   slots by a third equivalent operation associated with fewer than all of the issue slots

8   associated with the functional unit, thereby allowing one or more of the rest of the issue

9   slots to be used by the second operation.

1   24. (Previously amended) The processor-readable medium of claim 23, further

2   containing processor-executable instructions for analyzing the first operation and external

3   information to determine whether the first operation can be replaced by the third

4   equivalent operation.

1   25. (Previously amended) The processor-readable medium of claim 23, wherein

2   the third equivalent operation is associated with only one issue slot.

1   26. (Previously amended) The processor-readable medium of claim 23, further

2   containing processor-executable instructions for:

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3   determining a number of input registers and a number of output registers that are

4   used by the first operation; and

5   when the first operation uses at most two input registers and one output register,

6   replacing the first operation with the third equivalent operation associated with only one

7   issue slot.

1   27-28. (cancelled)

1   29. (Previously amended) The processor-readable medium of claim 23, wherein

2   the first operation is a shuffle operation.

1   30. (Previously amended) The processor-readable medium of claim 23, wherein

2   the first operation is a floating point operation.

1   31. (original) A processor-readable medium containing processor-executable

2   instructions for:

3   receiving a superoperation of a type typically associated with at least two issue

4   slots of a functional unit of a programmable processor;

5   determining a number of input registers and a number of output registers that are

6   used by the superoperation; and

7   when the superoperation uses at most two input registers and one output register,

8   replacing the superoperation with an equivalent operation associated with only one issue

9   slot.

1   32. (original) The processor-readable medium of claim 31, further containing

2   processor-executable instructions for:

3   identifying any source operations that produce a result affecting a result of the

4   superoperation;

5   placing commands for the source operations in instruction words;

6   selecting an earliest instruction word from a set of instruction words after the

7   instruction words in which commands for the source operations have already been

8   placed; and

9 determining whether an instruction word can be constructed that contains any

10 commands already included in the earliest instruction word in addition to a command for

11 the superoperation.

1 33. (original) The processor-readable medium of claim 32, further containing

2 processor-executable instructions for:

3 when an instruction word that contains any commands already included in the

4 earliest instruction word in addition to the command for the superoperation cannot be

5 constructed, selecting a subsequent instruction word; and

6 determining whether an instruction word that contains any commands already

7 included in the earliest instruction word in addition to the command for the

8 superoperation can be constructed using the subsequent instruction word.

1 34. (original) The processor-readable medium of claim 31, wherein the

2 superoperation is a shuffle operation.

1 35. (original) The processor-readable medium of claim 31, wherein the

2 superoperation is a floating point operation.

1 36. (Previously amended) A processor-readable medium containing processor-

2 executable instructions for:

3 determining whether a first instruction that is typically associated with at least two

4 issue slots in a functional unit of a processor can be executed using fewer than the at least

5 two issue slots; and

6 when the first instruction can be executed using fewer than the at least two issue

7 slots, replacing the first instruction with a second equivalent instruction that is associated

8 with fewer than the at least two issue slots thereby allowing one or more of the rest of the

9 issue slots to be used by a third instruction.

1 37. (Previously amended) The processor-readable medium of claim 36, further

2 containing processor-executable instructions for analyzing the first instruction and

3 external information to determine whether the first instruction can be executed using

4 fewer than the at least two issue slots.

1   38. (Previously amended) The processor-readable medium of claim 36, further

2   containing processor-executable instructions for:

3   determining a number of input registers and a number of output registers that are

4   used by the first instruction; and

5   when the first instruction uses at most two input registers and one output register,

6   replacing the first instruction with the second instruction, the second instruction being

7   associated with a single issue slot.

1   39-40. (cancelled)

1   41. (Previously amended) The processor-readable medium of claim 36, wherein

2   the second instruction is associated with two or more issue slots.

1   42. (Previously amended) The processor-readable medium of claim 36, wherein

2   the first instruction is a shuffle operation.

1   43. (Previously amended) The processor-readable medium of claim 36, wherein

2   the first instruction is a floating point operation.

1   44.   (cancelled)

1   45.   (cancelled)

1   46.   (cancelled)

1   47.   (cancelled)